Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A method for selectively etching a high dielectric constant layer over a silicon substrate, comprising:

placing the silicon substrate into an etch chamber;

providing an etchant gas into the etch chamber, wherein the etchant gas comprises BCl_3, an inert diluent, and Cl_2, wherein the flow ratio of the inert diluent to BCl_3 is between 2:1 and 1:2, and wherein the flow ratio of BCl_3 to Cl_2 is between 2:1 and 20:1; and

generating a plasma from the etchant gas to selectively etch the high dielectric constant layer.

2. (Original) The method, as recited in claim 1, further comprising maintaining the wafer temperature below 150° C during the etching.

3. (Original) The method, as recited in claim 2, further comprising providing a DC bias of less than 5 volts.

4. (Original) The method, as recited in claim 3, further comprising maintaining a pressure within the chamber to less than 40 mTorr during the etch.

5. (Original) The method, as recited in claim 4, wherein the generating a plasma comprises providing more than 700 Watts of Transformer Coupled Power into the etch chamber to energize the etchant gas.

6. (Original) The method, as recited in claim 5, wherein the inert diluent is argon.

7. (Original) The method, as recited in claim 6, wherein the etchant gas consists essentially of BCl_3, argon, and Cl_2.

8. (Original) The method, as recited in claim 7, wherein the selectivity for etching the high dielectric constant layer with respect to silicon is greater than 4:1.

9. (Original) The method, as recited in claim 8, where the etch rate of the high dielectric constant layer is between 50-150 Å/minute.

10. (Original) The method, as recited in claim 9, wherein the high dielectric constant layer has a dielectric constant of at least 8.

11. (Original) The method, as recited in claim 1, further comprising providing a DC bias with an absolute value of less than 5 volts.

12. (Original) The method, as recited in claim 1, further comprising maintaining a pressure within the chamber to less than 40 mTorr during the etch.

13. (Original) The method, as recited in claim 1, wherein the inert diluent is argon.

14. (Original) The method, as recited in claim 1, wherein the etchant gas consists essentially of BCl_3, argon, and Cl_2.

15. (Original) The method, as recited in claim 1, wherein the selectivity for etching the high dielectric constant layer with respect to silicon is greater than 4:1.

16. (Original) The method, as recited in claim 1, where the etch rate of the high dielectric constant layer is between 50-150 Å/minute.

17. (Original) The method, as recited in claim 1, wherein the high dielectric constant layer has a dielectric constant at least 8.

18. (Original) A method for forming a semiconductor device, comprising:

forming a high dielectric constant layer over a substrate;

forming a poly-silicon layer over the high dielectric constant layer;

forming a patterned mask over the poly-silicon layer;

etching a feature into the poly-silicon layer through the patterned mask;

etching the high dielectric constant layer to expose the substrate not under the patterned mask, comprising the steps of:

providing an etchant gas, wherein the etchant gas comprises BCl_3, an inert diluent, and Cl_2, wherein the flow ratio of the inert diluent to BCl_3 is between 2:1 and 1:2, and wherein the flow ratio of BCl_3 to Cl_2 is between 2:1 and 20:1; and

generating a plasma from the etchant gas to selectively etch the high dielectric constant layer; and

performing an ion implantation into the exposed substrate.

19. (Original) The method, as recited in claim 18, further comprising maintaining the wafer temperature below 150° C during the etching.

20. (Original) The method, as recited in claim 18, further comprising providing a DC bias with an absolute value of less than 5 volts.